AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A phase lock loop device comprising:

~~a reference frequency:~~

a voltage controlled oscillator (VCO) having a frequency *Fosc*;

a loop filter coupled to said VCO;

a phase detector coupled to said loop filter and said VCO;

a frequency ratio generator ~~means,~~ FRG coupled to said phase detector, said FRG receiving a reference signal having a reference frequency *Fref* ~~for~~ and generating a comparison frequency signal G1 ~~desired~~ whose dominant frequency component *Fc* is a desired frequency *Fosc* based on a fraction expansion of ~~the~~ a ratio *P/Q* of said desired frequency ~~to the~~ *Fosc* and said reference frequency *Fref*,

wherein *P* and *Q* are integer numbers, said ratio *P/Q* being realized according to a mathematical expression $1 \pm 1/p_1 \pm 1/p_2 \pm \ldots 1/p_n$, or realized according to a mathematical expression $1 \pm 1/q_1 \cdot \{1 \pm 1/q_2 \cdot [\ldots(1 \pm \ldots 1/q_m)))\ldots]\}$, or realized according to a combination of said mathematical expressions,

wherein n, m, and coefficients $p_1, p_2, \ldots, p_n, q_1, q_2, \ldots, q_m$ are positive integer numbers, and

whereby all additions in said mathematical expressions are realized by an upper side-band SSB mixer, all subtractions are realized by a lower-side-band SSB mixer, and all fractions $1/p_1$ through $1/p_n$ and $1/q_1$ through $1/q_m$ are realized by frequency dividers.

2. (New) The device of claim 1, wherein said fraction expansion of said ratio *P/Q* is optimized for best spectral purity at the vicinity of said VCO output signal frequency *Fosc*, whereas said fraction expansion is also chosen to have terms that are most favorable for optimum hardware realization.

3. (New) The device of claim 1, wherein one or more of the ratios of said frequency dividers is programmable, and the sideband of one or more of said SSB mixers is selected to be either the upper sideband (USB) for additions or the lower sideband (LSB) for subtractions.

4. (New) The device of claim 3, wherein a plurality of equidistant discrete frequency steps continuous within a determined frequency range are programmed such that each step has a different dominant frequency *Fc* selectable among said plurality of equidistant discrete frequency steps within said determined frequency range.

5. (New) The device of claim 1, wherein said comparison frequency signal is a complex signal consisting of two constituent components being an in-phase component and a quadrature component having a dominant frequency *Fc*,

wherein said VCO output signal is split into a complex VCO output signal having two constituent components being an in-phase component and a quadrature component having a dominant frequency *Fosc*; and

wherein said complex signal having a dominant frequency *Fc* is phase locked to said complex VCO output signal having a frequency *Fosc* by using said phase detector based on a SSB mixer to generate a phase detector output provided to said loop filter..

6. (New) The device of claim 1, further comprising:

a frequency divider for dividing the frequency of said VCO output signal by an integer *M* to provide a signal of frequency *Fosc/M* to said phase detector,

wherein said signal of frequency *Fosc/M* is phase locked with said reference signal having a dominant frequency component $Fc = P/Q \cdot Fref$ through said phase detector to generate a phase detector output such that said frequency *Fosc/M* becomes substantially equal to said dominant frequency *Fc* satisfying the relationship $Fosc = M \cdot Fc = M \cdot P/Q \cdot Fref$.

7. (New) The device of claim 1, wherein:

said reference frequency *Fref* is a bi-level (digital) signal having a dominant frequency;

said SSB mixer is a complex bi-level (digital) mixer;

said phase detector is a bi-level (digital) phase detector;

said VCO output signal is sliced into a bi-level (digital) signal having said dominant frequency *Fosc*.

8. (New) The device of claim 1, wherein the phase of said comparison frequency signal generated having the dominant frequency *Fc* is programmed in discrete equal steps to control the phase of said VCO output signal in discrete equal steps covering a full period of 360° of one cycle of said VCO output signal.

9. (New) The device of claim 1, further comprising:

a second Frequency Ratio Generator FRG2,

wherein said reference frequency *Fref* is received at an input of said FRG2 to produce a second output signal G2 at an output of said FRG2 having a dominant frequency $Fg2 = U/V \cdot Fref$, *U/V*, being a ratio of two positive integers,

wherein said VCO output signal is offset by said dominant frequency *Fg2* of said second output signal G2 either in the positive sense using a USB mixer or in the negative sense using an LSB mixer to produce an offset VCO signal having a dominant frequency of $Fosc \pm Fg2$,

wherein said signal G1 has said dominant frequency *Fc* phase locked with said offset VCO signal having a frequency $Fosc \pm Fg2$ through said phase detector to generate a phase detector output such that said frequency $Fosc \pm Fg2$ becomes substantially equal to said dominant frequency *Fc* satisfying the relationship $Fosc = Fc \pm Fg2 = (P/Q \pm U/V) \cdot Fref$;

a second loop filter for filtering said phase detector output to generate a second loop filter output; and

a VCO output signal generated by transmitting said second loop filter output to a tuning input of said VCO.

10. (New) A method of phase-lock loop (PLL) frequency synthesis, the method comprising:

receiving a reference signal having a reference frequency *Fref* in a frequency ratio generator FRG;

generating through a voltage controlled oscillator (VCO) a VCO output signal having a frequency *Fosc*;

coupling said VCO output signal to a first input of a phase detector;

filtering an output of said phase detector to obtain a filtered signal for coupling said filtered signal to said VCO;

coupling said reference signal from said FRG to a second input of said phase detector, said FRG generating a comparison frequency signal G1 whose dominant frequency component *Fc* is a desired frequency *Fosc* based on a fraction expansion of a ratio *P/Q* of said desired frequency *Fosc* and said reference frequency *Fref*,

wherein *P* and *Q* are integer numbers, said ratio *P/Q* being realized according to a mathematical expression $1 \pm 1/p_1 \pm 1/p_2 \pm \ldots 1/p_n$, or realized according to a mathematical expression $1 \pm 1/q_1 \cdot \{1 \pm 1/q_2 \cdot [\ldots (1 \pm 1/q_m))) \ldots]\}$, or realized according to a combination of said mathematical expressions,

wherein n, m and coefficients $p_1, p_2, \ldots, p_n$, $q_1, q_2, \ldots, q_m$ are positive integer numbers, and

whereby all additions in said mathematical expressions are realized by upper side-band SSB mixing, all subtractions are realized by lower-side-band SSB mixing, and all fractions $1/p_1$ through $1/p_n$ *and* $1/q_1$ *through* $1/q_m$ are realized by frequency division.

11. (New) The method of claim 10, further comprising:

optimizing a fraction expansion of said ratio P/Q for best spectral purity at the vicinity of said VCO output signal frequency *Fosc*,

optimizing said fraction expansion for most favorable hardware realization.

12. (New) The method of claim 10, further comprising:

controlling said dominant frequency *Fc* of said generated signal G1 in order to obtain a plurality of desired frequencies by programming one or more of said coefficients of said fraction expansion by programming one or more of the ratios of said frequency divisions, and by selecting the sidebands of one or more of said SSB mixing to be either the upper sideband (USB) for additions or the lower sideband (LSB) for subtractions.

13. (New) The method of claim 12, further comprising:

programming a plurality of equidistant discrete frequency steps that are continuous within a determined frequency range, each step having a different dominant

frequency *Fc* selectable among the plurality of said discrete frequency steps within said determined frequency range.

14. (New) The method of claim 10, further comprising:

maximizing a loop bandwidth by selecting combinations of said coefficients of said fraction expansion and said ratios of said frequency division, and said additions by upper side-band SSB mixing (USB) and said subtractions by lower-side-band SSB mixing (LSB) such that a closest significant spurious spectral component to said dominant frequency *Fc* is at an offset frequency from *Fc* that is substantially greater than a frequency step size within a determined frequency range, such that the loop bandwidth determined by said loop filter is substantially greater than said frequency step size.

15. (New) The method of claim 10, wherein said comparison frequency signal is a complex signal consisting of two constituent components being an in-phase component and a quadrature component having a dominant frequency *Fc*;

and further comprising:

splitting said VCO output signal into a complex VCO output signal having two constituent components being an in-phase component and a quadrature component having a dominant frequency *Fosc*; and

phase locking said comparison frequency signal having said dominant frequency *Fc* with said complex VCO output signal having a frequency *Fosc* using said complex

phase detector based on SSB mixing such that a phase detector output is provided to said loop filter.

16. (New) The method of claim 10, further comprising:

dividing the frequency of said VCO output signal by an integer M to obtain a signal of frequency $Fosc/M$ to said phase detector;

phase locking said signal of frequency $Fosc/M$ with said reference signal having a dominant frequency component $Fc = P/Q \cdot Fref$ through said phase detector generating a phase detector output such that said frequency $Fosc/M$ becomes substantially equal to said dominant frequency Fc satisfying the relationship $Fosc = M \cdot Fc = M \cdot P/Q \cdot Fref$.

17. (New) The method of claim 10, further comprising:

controlling the phase of said VCO output signal by controlling the phase of said comparison frequency signal having a dominant frequency Fc by programming said phase of said comparison frequency signal in discrete equal steps covering a full period of 360° of one cycle of said VCO output signal.

18. (New) The method of claim 10, further comprising:

receiving said reference signal having a reference frequency $Fref$ at an input of a second Frequency Ratio Generator (FRG2) to produce a second output signal G2 at an output of said FRG2 having a dominant frequency $Fg2 = U/V \cdot Fref$, U/V, being a ratio of two positive integers;

offsetting said VCO output signal by said dominant frequency *Fg2* of said second output signal G2 either in the positive sense using USB mixing or in the negative sense using LSB mixing, producing an offset VCO signal having the dominant frequency of *Fosc±Fg2*;

phase-locking said generated signal G1 having said dominant frequency *Fc* with said offset VCO signal having a frequency *Fosc±Fg2* through said phase detector, generating a phase detector output such that said frequency *Fosc±Fg2* becomes substantially equal to said dominant frequency *Fc* satisfying the relationship $Fosc = Fc \pm Fg2 = (P/Q \pm U/V) \cdot Fref$;

filtering said phase detector output through a second loop filter generating a second loop filter output; and

transmitting said second loop filter output to a tuning input of said VCO producing said VCO output signal.

19. (New) A Frequency Ratio Generator (FRG) frequency translation device, comprising:

an input signal having a frequency *Fin;* and

an output signal having a dominant frequency $Fg = P/Q \cdot Fin$, *P/Q* being a ratio of two positive integers equal to one of a first fraction expansion $1 \pm 1/p_1 \pm 1/p_2 \pm \ldots 1/p_n$, a second fraction expansion $1 \pm 1/q_1 \cdot \{1 \pm 1/q_2 \cdot [\ldots (1 \pm 1/q_m))) \ldots]\}$, or a mathematical expression which is a combination of said first and second fraction expansions, *m*, *n* and coefficients

$p_1, p_2, \ldots, p_n$, $q_1, q_2, \ldots, q_m$ being positive integer numbers, all additions being realized by an upper side-band SSB mixer (USB), all subtractions by a lower-side-band SSB mixer (LSB) and all the fractions $1/p_1$ through $1/p_n$ and $1/q_1$ through $1/q_m$ by a frequency divider.

20. (New) The device of claim 19, further comprising:

a filter coupled to said output signal.

21. (New) A method of Frequency Ratio Generation (FRG) frequency translation, the method comprising:

receiving an input signal having a frequency *Fin;*

generating a signal whose dominant frequency component *Fg* is equal to a ratio *P/Q* multiplied by said frequency *Fin*,

wherein *P* and *Q* are integer numbers,

said ratio *P/Q* being realized according to a mathematical expression $1 \pm 1/p_1 \pm 1/p_2 \pm \ldots 1/p_n$, or realized according to a mathematical expression $1 \pm 1/q_1 \cdot \{1 \pm 1/q_2 \cdot [\ldots (1 \pm 1/q_m))) \ldots]\}$, or realized according to a combination of said mathematical expressions;

wherein *n, m* and coefficients $p_1, p_2, \ldots, p_n$, $q_1, q_2, \ldots, q_m$ are positive integer numbers, and

whereby all additions in said mathematical expressions are realized by upper side-band SSB mixing, all subtractions are realized by lower-side-band SSB mixing and all fractions $1/p_1$ through $1/p_n$ *and* $1/q_1$ *through* $1/q_m$ are realized by frequency division.

22. (New) The method of claim 21, further comprising:

filtering said generated signal .

23. (New) A phase-lock loop (PLL) frequency synthesizer device, comprising:

a Frequency Ratio Generator (FRG) frequency translator, comprising:

an input signal having a frequency *Fin;* and

an output signal having a dominant frequency $Fg = P/Q \cdot Fin$, P/Q being a ratio of two positive integers equal to one of a first fraction expansion $1 \pm 1/p_1 \pm 1/p_2 \pm \ldots 1/p_n$, a second fraction expansion $1 \pm 1/q_1 \cdot \{1 \pm 1/q_2 \cdot [\ldots (1 \pm 1/q_m))) \ldots]\}$, or a mathematical expression which is a combination of said first and second fraction expansions, m, n and coefficients $p_1, p_2, \ldots, p_n$ $q_1, q_2, \ldots, q_m$ being positive integer numbers, all additions being realized by using an upper side-band SSB mixer (USB), all subtractions by a lower-side-band SSB mixer (LSB) and all the fractions $1/p_1$ through $1/p_n$ and $1/q_1$ through $1/q_m$ by a frequency divider;

an input reference signal having a reference frequency *Fref*;

a voltage controlled oscillator (VCO) output signal having a frequency *Fo* coupled to said input of said FRG to produce said output signal at an output of said FRG having a dominant frequency $Fg = R/S \cdot Fo$, R/S being a ratio of two positive integers,

wherein said output signal having said dominant frequency *Fg* is phase locked with said input reference signal having a reference frequency *Fref* through a phase detector to generate a phase detector output such that said frequency *Fg* becomes substantially equal to said reference frequency *Fref* satisfying the relationship $Fo = S/R \cdot Fref$;

a loop filter for filtering said phase detector output to generate a loop filter output; and

a VCO output signal generated by transmitting said loop filter output to a tuning input of said VCO.

24. (New) A method of phase-lock loop (PLL) frequency synthesis using a Frequency Ratio Generator (FRG) frequency translation, the method comprising:

receiving an input signal having a frequency *Fin* at an input of said FRG;

producing an output signal at an output of said FRG having a dominant frequency $Fg = P/Q \cdot Fin$, *P/Q* being a ratio of two positive integers equal to one of a first fraction expansion $1 \pm 1/p_1 \pm 1/p_2 \pm \ldots 1/p_n$, a second fraction expansion $1 \pm 1/q_1 \cdot \{1 \pm 1/q_2 \cdot [\ldots (1 \pm 1/q_m))) \ldots]\}$, or a mathematical expression which is a combination of said first and second fraction expansions, *m*, *n* and coefficients $p_1, p_2, \ldots, p_n$, $q_1, q_2, \ldots, q_m$ being positive integer numbers, realizing all additions by upper side-band SSB mixing (USB), all subtractions by lower-side-band SSB mixing (LSB) and all the fractions $1/p_1$ through $1/p_n$ and $1/q_1$ through $1/q_m$ by frequency division; and

receiving an input reference signal having a reference frequency *Fref*;

generating through a voltage controlled oscillator (VCO) a VCO output signal having a frequency *Fo* and coupling it to said input of said FRG, thereby producing at said output of said FRG a translated output signal having a dominant frequency $Fg = R/S \cdot Fo$, *R/S* being a ratio of two positive integers;

phase locking said translated output signal having said dominant frequency *Fg* with said input reference signal having a reference frequency *Fref* through a phase detector, generating a phase detector output such that said frequency *Fg* becomes substantially equal to said reference frequency *Fref* satisfying the relationship $Fo = S/R \cdot Fref$;

filtering said phase detector output through a loop filter generating a loop filter output; and

transmitting said loop filter output to a tuning input of said VCO producing said VCO output signal.